REMARKS

This is a full and timely response to the outstanding nonfinal Office Action mailed Nov. 29, 2005. Applicants submit that claims 1-38, 40-45 are canceled hereby; claim 39 is amended hereby, claims 49 and 50 is newly added depending from claim 46, and claims 46-48 are remained unchanged. Reconsideration and allowance of the application and presently pending claims 39, and 46-48 are respectfully requested. Supports to the amendments can be found in Paragraph 0052 and the drawings, i.e., FIG. 9. Supports to the newly added claims 49 and 50 can be found in FIGS. 5G and 7G, and throughout the specification.

Discussion of Office Action Rejections

The Office Action rejected claims 39-42 and 46-48 under 35 U.S.C. 102(b) as being anticipated by Voldman et al. US Patent 6,015,993.

In response to the rejection to claims claims 39-42 and 46-48 under 35 U.S.C. 102(b) as being anticipated by Voldman et al. US Patent 6,015,99, Applicants have amended claim 39 and canceled claims 40-42, and hereby otherwise traverses this rejection. As such, Applicant submits that claims 39, and 46-48 are now in condition for allowance.

With respect to claim 39, as currently amended, recites in part:

A method of forming a non-gate diode of a SOI, comprising:

...forming a P-type heavily doped region and an N-type heavily doped region in the well region, the P-type heavily doped region is configured between and connects the lightly doped P-type region and one isolating structure, and the N-type heave doped region is configured between and connects the lightly doped N-type region and the other isolating structure.

Applicant submits that such a method of forming a non-gate diode of a SOI, as set forth in claim 39 as amended, is neither taught, disclosed, nor suggested by Voldman, or any of the other cited references, taken alone or in combination.

Ayres US Patent 5,947,578 fails to disclose, teach or suggest a step of "forming a P-type heavily doped region and an N-type heavily doped region in the well region, wherein the **P-type heavily doped region is configured between and connects the lightly doped region and one isolating structure, and the N-type heave doped region is configured between and connects the lightly doped region and the other isolating structure**" which is required for the method as set forth in claim 39 (Emphasis added.). Therefore, claim 39 as currently amended should not be considered as being anticipated by Voldman et al. US Patent 6,015,99 or any of the other cited references, taken alone or in combination, and is submitted as allowable.

With respect to claim 46, as original, recites in parts:

A method of forming a non-gate diode in a CMOS process, comprising:

providing a substrate having a well region therein;

... each second type doped region is separated from the first type doped region by the well.

Applicant submits that such a method of forming a non-gate diode in a CMOS process, as set forth in claim 46 as original, is neither taught, disclosed, nor suggested by Voldman, or any of the other cited references, taken alone or in combination.

Voldman teaches, in FIG. 7, a substrate. However, Voldman fails to teach a substrate having a well region therein, that is required for the present invention, as set forth in claim 46. The well region of Voldman is formed in the insulating layer. The Examiner alleged that in this case, the buried oxide layer 156 is a substrate having a well region therein. However, the item 156 is an insulator layer (Column 4, lines 23). One of ordinary skill in the art should understand that an insulator layer is not suitable to have a well region by doping. Therefore, item 156 should not be construed as a substrate having a well region therein.

Accordingly, the present invention as set forth in claim 46 is submitted novel, unobvious and patentable over Voldman, or any of the other cited references, taken alone or in combination, and thus should be allowable.

If independent claim 46 is allowable over the prior art of record, then its dependent claims 47-50 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 46. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 39, 46-50 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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